2Pai Semi

4.0 kV rms/6.0 kV rms Penta-Channel Digital Isolators

Data Sheet **π150/π151/π152**

FEATURES

- Ultra low power consumption:
  - 0.38mA/Ch (0~500Kbps, Supply voltage: 3.0~5.5V)
- High data rate: π15xA: 600Mbps
  - π15xM: 10Mbps
  - π15xU: 150kbps
- High common-mode transient immunity: 45 kV/μs typical
- High robustness to radiated and conducted noise
- Low propagation delay:
  - 4.4 ns maximum for 5 V operation
  - 5.2 ns maximum for 3.3 V operation
- Isolation voltages:
  - π15xx4: AC 4000Vrms
  - π15xx6: AC 6000Vrms
- Safety and regulatory approvals (Pending)
  - UL recognition:
    - 4000Vrms/6000Vrms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
  - VDE certificate of conformity
    - DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 565V peak/849V peak
  - CQC certification per GB4943.1-2011
- 3.0 V to 5.5 V level translation
- AEC-Q100 qualification
- Wide temperature range: -40°C to 125°C
- 16-lead, RoHS-compliant, (W)SOIC package
- Unused input pin should be connected to default

APPLICATIONS

- General-purpose multichannel isolation
- Industrial field bus isolation

GENERAL DESCRIPTION

The π1xxx are 2PaiSemi digital isolators product family. By using maturated standard semiconductor CMOS technology and innovative design, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated isolators. The maximum propagation delay is 3.6 ns with a pulse width distortion of less than 0.3 ns at 5.0V operation. Channel matching is tight at 0.4 ns maximum. The π1xxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 4.0 kV rms to 8.0 kV rms and the data rate from 150Kbps up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

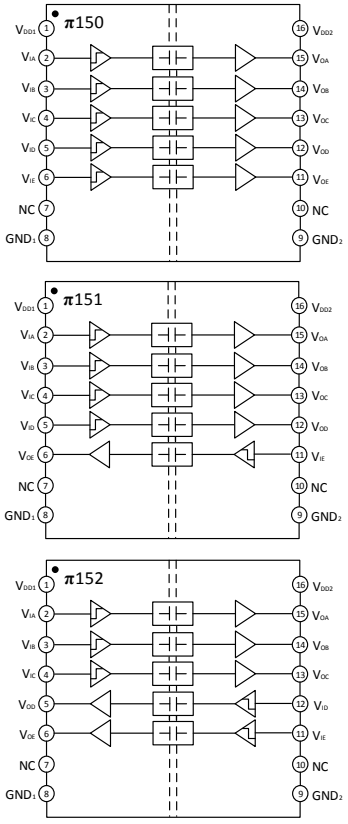

Figure1. π150/π151/π152 functional Block Diagram

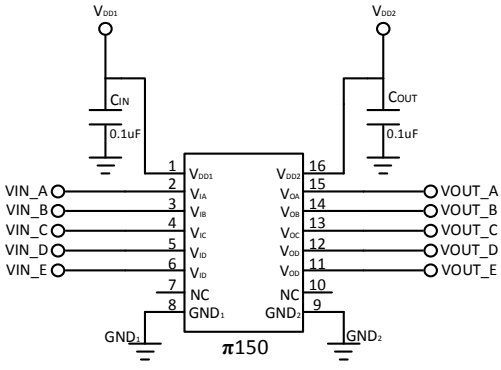

Figure2. π150 typical Application Circuit

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V. Minimum/maximum specifications apply over the entire recommended operation range of 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals and C_L = 0 pF.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
π15xA						
Pulse Width	PW			1.6	ns	Within pulse width distortion (PWD) limit
Max Data Rate		600			Mbps	Within PWD limit
π15xM						
Pulse Width	PW			100	ns	Within pulse width distortion (PWD) limit
Max Data Rate		10			Mbps	Within PWD limit
π15xU						
Pulse Width	PW			6.6	µs	Within pulse width distortion (PWD) limit
Max Data Rate		150			Kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	2.6	3.6	4.6	ns	50% input to 50% output
Pulse Width Distortion	PWD	0	0.3	0.4	ns	|tPLH − tPHL|
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			0.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0	0.4	ns	
Opposing Direction	t_{PSKOD}		0	0.4	ns	
Jitter			50		ps p-p	See the Jitter Measurement section
			8		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}			3.6	V	
Logic Low	V_{IL}	1.4			V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −4 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.1	0.2	V	I_{Ox}[1] = 4 mA, V_{Ix} = V_{IxL}[3]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						C_L = 0 pF
π150	$I_{DD1 (Q)}$	68	85	102	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	472	590	708	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	68	85	102	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	477	597	717	µA	V_I[4] = 1 (N0), 0 (N1)[5]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
π151	$I_{DD1 (Q)}$	269	337	405	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	280	351	422	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	265	332	399	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	269	337	405	µA	V_I[4] = 1 (N0), 0 (N1)[5]
π152	$I_{DD1 (Q)}$	269	337	405	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	280	351	422	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	265	332	399	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	269	337	405	µA	V_I[4] = 1 (N0), 0 (N1)[5]
Dynamic Supply Current						C_L = 0 pF
Dynamic Input	$I_{DDI (D)}$	10	13	16	µA /Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$	117	147	177	µA /Mbps	Inputs switching, 50% duty cycle
Under voltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}	2.35	2.62	2.88	V	
Negative V_{DDx} Threshold	V_{DDxUV-}	2.17	2.42	2.66	V	
V_{DDx} Hysteresis	V_{DDxUVH}	0.17	0.19	0.20	V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		0.7		ns	10% to 90%
Common-Mode Transient Immunity[6]	$\|CM_H\|$		45		kV/µs	$V_{Ix} = V_{DDx}$, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$		45		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

Notes:
[1] I_{Ox} is the Channel x output current, where x = A, B, C, D or E.
[2] V_{IxH} is the input side logic high voltage.
[3] V_{IxL} is the input side logic low voltage.
[4] V_I is the input voltage.
[5] N0 is the π150xx0/π151xx0/π152xx0 models, and N1 is the π150xx1/π151xx1/π152xx1 models. See the Ordering Guide.
[6] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining the voltage output $V_O > 0.8\ V_{DDx}$. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 2. Total Supply Current vs. Data Throughput (C_L = 0 pF)

		150 Kbps			10 Mbps			150 Mbps			
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SUPPLY CURRENT											
π150A											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π151A											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π152A											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA

Parameter	Symbol	150 Kbps Min	150 Kbps Typ	150 Kbps Max	10 Mbps Min	10 Mbps Typ	10 Mbps Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
π150M											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π151M											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π152M											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
SUPPLY CURRENT											
π150U											
Supply Current Side 1	I_{DD1}										µA
Supply Current Side 2	I_{DD2}										µA
π151U											
Supply Current Side 1	I_{DD1}										µA
Supply Current Side 2	I_{DD2}										µA
π152U											
Supply Current Side 1	I_{DD1}										µA
Supply Current Side 2	I_{DD2}										µA

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION.

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operation range: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF and CMOS signal levels, unless otherwise noted. Supply currents are specified with 50% duty cycle signals and C_L = 0 pF.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
π15xA						
Pulse Width	PW			1.6	ns	Within pulse width distortion (PWD) limit
Max Data Rate		600			Mbps	Within PWD limit
π15xM						
Pulse Width	PW			100	ns	Within pulse width distortion (PWD) limit
Max Data Rate		10			Mbps	Within PWD limit
π15xU						
Pulse Width	PW			6.6	µs	Within pulse width distortion (PWD) limit
Max Data Rate		150			Kbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}	3.4	4.4	5.4	ns	50% input to 50% output
Pulse Width Distortion	PWD	0	0.32	0.39	ns	|tPLH − tPHL|
Change vs. Temperature			1.5		ps/°C	
Propagation Delay Skew	t_{PSK}			0.5	ns	Between any two units at the same temperature, voltage, and load
Channel Matching						
Codirectional	t_{PSKCD}		0	0.4	ns	
Opposing Direction	t_{PSKOD}		0	0.4	ns	
Jitter			66		ps p-p	See the Jitter Measurement section
			11		ps rms	See the Jitter Measurement section
DC SPECIFICATIONS						
Input Threshold Voltage						
Logic High	V_{IH}			2.4	V	
Logic Low	V_{IL}	0.9			V	
Output Voltage						
Logic High	V_{OH}	V_{DDx} − 0.1	V_{DDx}		V	I_{Ox}[1] = −20 µA, V_{Ix} = V_{IxH}[2]
		V_{DDx} − 0.2	V_{DDx}		V	I_{Ox}[1] = −2 mA, V_{Ix} = V_{IxH}[2]
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox}[1] = 20 µA, V_{Ix} = V_{IxL}[3]
			0.1	0.2	V	I_{Ox}[1] = 2 mA, V_{Ix} = V_{IxL}[3]
Input Current per Channel	I_I	−10	+0.01	+10	µA	0 V ≤ V_{Ix} ≤ V_{DDx}
Quiescent Supply Current						C_L = 0 pF
π150	$I_{DD1 (Q)}$	67	84	101	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	484	605	726	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	67	84	101	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	488	610	732	µA	V_I[4] = 1 (N0), 0 (N1)[5]

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
π151	$I_{DD1 (Q)}$	274	343	412	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	284	355	426	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	272	340	408	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	276	346	416	µA	V_I[4] = 1 (N0), 0 (N1)[5]
π152	$I_{DD1 (Q)}$	274	343	412	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD2 (Q)}$	284	355	426	µA	V_I[4] = 0 (N0), 1 (N1)[5]
	$I_{DD1 (Q)}$	272	340	408	µA	V_I[4] = 1 (N0), 0 (N1)[5]
	$I_{DD2 (Q)}$	276	346	416	µA	V_I[4] = 1 (N0), 0 (N1)[5]
Dynamic Supply Current						C_L = 0 pF
Dynamic Input	$I_{DDI (D)}$		8		µA /Mbps	Inputs switching, 50% duty cycle
Dynamic Output	$I_{DDO (D)}$		53		µA /Mbps	Inputs switching, 50% duty cycle
Undervoltage Lockout	UVLO					
Positive V_{DDx} Threshold	V_{DDxUV+}	2.35	2.62	2.88	V	
Negative V_{DDx} Threshold	V_{DDxUV-}	2.17	2.42	2.66	V	
V_{DDx} Hysteresis	V_{DDxUVH}	0.17	0.19	0.20	V	
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		0.7		ns	10% to 90%
Common-Mode Transient Immunity[6]	$\|CM_H\|$		45		kV/µs	V_{Ix} = V_{DDx}, V_{CM} = 1000 V, transient magnitude = 800 V
	$\|CM_L\|$		45		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V

Notes:
[1] I_{Ox} is the Channel x output current, where x = A, B, C, D or E.
[2] V_{IxH} is the input side logic high voltage.
[3] V_{IxL} is the input side logic low voltage.
[4] V_I is the input voltage.
[5] N0 is the π150xx0/π151xx0/π152xx0 models, and N1 is the π150xx1/π151xx1/π152xx1 models. See the Ordering Guide.
[6] $|CM_H|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V_{DDx}. $|CM_L|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining V_O > 0.8 V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

Table 4. Total Supply Current vs. Data Throughput (C_L = 0 pF)

		150 Kbps			10 Mbps			150 Mbps			
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
π150A											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π151A											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π152A											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA

Parameter	Symbol	150 Kbps Min	150 Kbps Typ	150 Kbps Max	10 Mbps Min	10 Mbps Typ	10 Mbps Max	Min	Typ	Max	Unit
SUPPLY CURRENT											
π150M											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π151M											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
π152M											
Supply Current Side 1	I_{DD1}										mA
Supply Current Side 2	I_{DD2}										mA
SUPPLY CURRENT											
π150U											
Supply Current Side 1	I_{DD1}										µA
Supply Current Side 2	I_{DD2}										µA
π151U											
Supply Current Side 1	I_{DD1}										µA
Supply Current Side 2	I_{DD2}										µA
π152U											
Supply Current Side 1	I_{DD1}										µA
Supply Current Side 2	I_{DD2}										µA

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5.
π15xx4

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		4000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	4.0	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	4.0	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		8	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

π15xx6

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		6000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (I01)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (I02)	8.3	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.3	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		14	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 6.

π12xx4

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		0.6		pF	f = 400Hz
Input Capacitance[2]	C_I		3.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		76		°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

[2]Input capacitance is from any input data pin to ground.

π12xx6

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		0.6		pF	f = 400Hz
Input Capacitance[2]	C_I		3.0		pF	
IC Junction to Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

[2]Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

See Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table7.

π15xx4

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified under CQC11-471543-2012

Single Protection, 4000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 400 V rms (565 V peak) Reinforced insulation at 200 V rms (283 V peak) IEC 60601-1 Edition 3.1: Basic insulation (1 MOPP), 250 V rms (354 V peak) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms mains, 400 V rms (565 V peak) Reinforced insulation at 300 V rms mains, 200 V secondary (283 V peak)	Basic insulation, V_{IORM} = 565 V peak, V_{IOSM} = 4615 V peak	GB4943.1-2011 Basic insulation at 770 V rms (1089 V peak) working voltage Reinforced insulation at 385 V rms (545 V peak)
File (pending)	File (pending)	File (pending)	File (pending)

Notes:

[1] In accordance with UL 1577, each π150x4/π151x4/π152x4 is proof tested by applying an insulation test voltage ≥ 4800 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-10, each π150x4/π151x4/π152x4 is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

π15xx6

UL (Pending)	CSA (Pending)	VDE (Pending)	CQC (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice 5A	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]	Certified under CQC11-471543-2012
Single Protection, 6000 V rms Isolation Voltage	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 830 V rms (1174 V peak) Reinforced insulation at 415 V rms (587 V peak) IEC 60601-1 Edition 3.1: Basic insulation (2 MOPP), 261 V rms (369 V peak) CSA 61010-1-12 and IEC 61010-1 third edition Basic insulation at 300 V rms mains, 830 V rms (1174 V peak) Reinforced insulation at 300 V rms mains, 200 V secondary (283 V peak)	Basic insulation, V_{IORM} = 849 V peak, V_{IOSM} = 7692 V peak Reinforced insulation, V_{IORM} =849 V peak, V_{IOSM} = 10 kV peak	GB4943.1-2011 Basic insulation at 830 V rms (1174 V peak) working voltage Reinforced insulation at 415 V rms (587 V peak)
File (pending)	File (pending)	File (pending)	File (pending)

Notes:

[1] In accordance with UL 1577, each π150x6/π151x6/π152x6 is proof tested by applying an insulation test voltage ≥ 7200 V rms for 1 sec.

[2] In accordance with DIN V VDE V 0884-10, each π150x6/π151x6/π152x6 is proof tested by applying an insulation test voltage ≥ 1592 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 8.

π15xx4

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to III	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, 100% production test, tini = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1059	V peak
Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	Vpd (m)	848	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		678	V peak
Highest Allowable Overvoltage		V_{IOTM}	5656	V peak
Surge Isolation Voltage Basic	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4615	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	1.64	W
Insulation Resistance at T_S	V_{IO} = 800 V	R_S	$>10^9$	Ω

π15xx6

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to IV	
For Rated Mains Voltage ≤ 600 V rms			I to III	
Climatic Classification			40/125/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	849	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, 100% production test, tini = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1592	V peak
Input to Output Test Voltage, Method A After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	Vpd (m)	1274	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		1019	V peak

Highest Allowable Overvoltage		V_{IOTM}	8484	V peak
Surge Isolation Voltage Basic	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	7692	V peak
Surge Isolation Voltage Reinforced	V peak = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10000	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.78	W
Insulation Resistance at T_S	V_{IO} = 800 V	R_S	>10^9	Ω

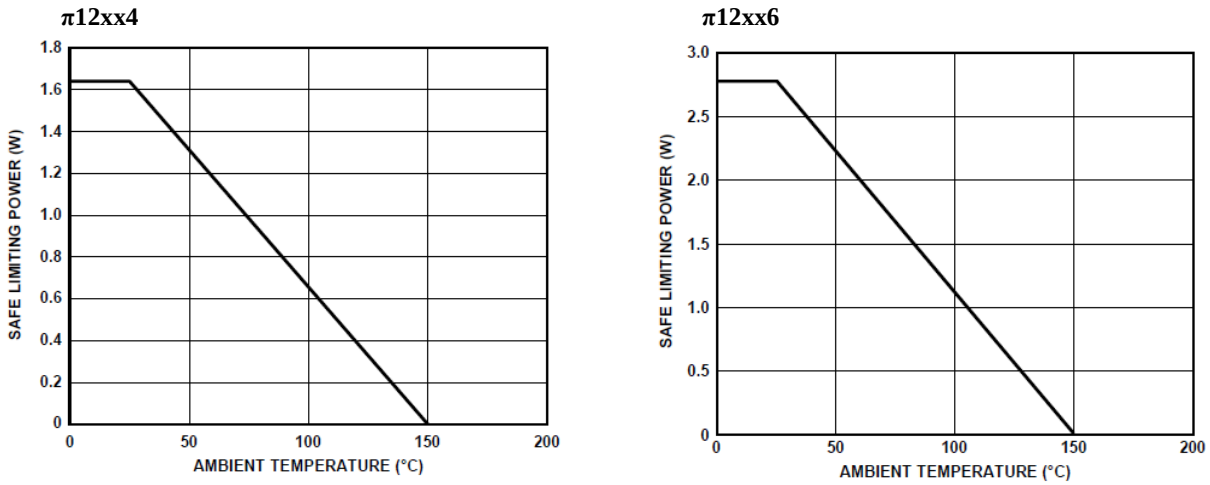


Figure3. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

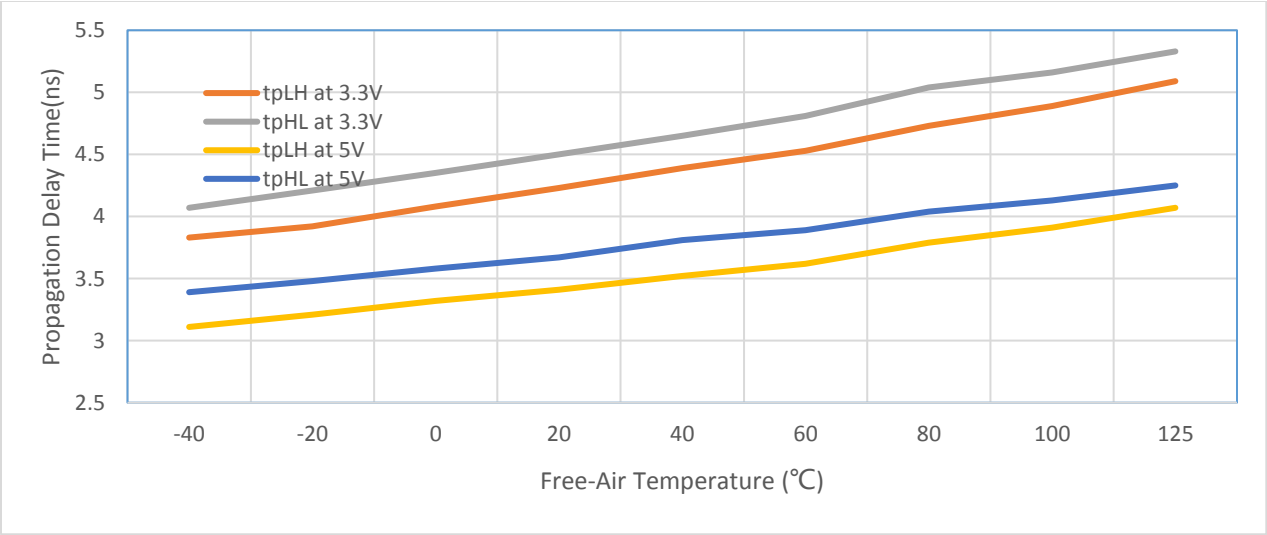


Figure Propagation Delay vs. Temperature at Various Voltages

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 9.

Parameter	Rating
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin[3]	
Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[4]	−150 kV/µs to +150 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:
[1] V_{DDI} is the input side supply voltage.
[2] V_{DDO} is the output side supply voltage.
[3] See Figure 3 for the maximum rated current values for various temperatures.
[4] Common-mode transients refer to the common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 10. Maximum Continuous Working Voltage[1]

π15xx4

Parameter	Rating	Constraint[2]
AC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Bipolar Waveform		
Basic Insulation	789 V peak	
Reinforced Insulation	403 V peak	
Unipolar Waveform		
Basic Insulation	909 V peak	
Reinforced Insulation	469 V peak	
DC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Basic Insulation	558 V peak	
Reinforced Insulation	285 V peak	

π15xx6

Parameter	Rating	Constraint[2]
AC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Bipolar Waveform		
Basic Insulation	849 V peak	
Reinforced Insulation	819 V peak	
Unipolar Waveform		
Basic Insulation	1698 V peak	
Reinforced Insulation	943 V peak	
DC VOLTAGE		Lifetime limited by package creepage maximum approved working voltage per IEC 60950-1
Basic Insulation	1157 V peak	
Reinforced Insulation	579 V peak	

Notes:

[1] Maximum continuous working voltage refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

[2] Insulation lifetime for the specified test condition is greater than 50 years.

Truth Tables

Table 11. π150/π151/π152 Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low (N0), V_{Ox} Output[1,2]	Default High (N1), V_{Ox} Output[1,2]	Test Conditions/Comments
Low	Powered[3]	Powered[3]	Low	Low	Normal operation
High	Powered[3]	Powered[3]	High	High	Normal operation
Don't Care[5]	Unpowered[4]	Powered[3]	Low	High	Fail-safe output
Don't Care[5]	Powered[3]	Unpowered[4]	High Impedance	High Impedance	

Notes:

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, D or E). V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of the given channel, respectively.

[2] N0 is the π150xx0/π151xx0/π152xx0 models; N1 is the π150xx1/π151xx1/π152xx1 models. See the Ordering Guide.

[3] Powered = Power Up ($V_{CC} \geq V_{DDxUV+}$), Power Down ($V_{CC} \geq V_{DDxUV-}$).

[4] Unpowered = Power Up ($V_{CC} < V_{DDxUV+}$), Power Down ($V_{CC} < V_{DDxUV-}$).

[5] Input pins (V_{Ix}) on the same side as an unpowered supply must be in a low state to avoid powering the device through its ESD protection circuitry.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

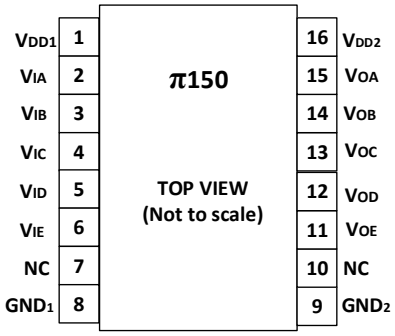


Figure4. π150 Pin Configuration

π150 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{ID}	Logic Input D.
6	V_{IE}	Logic Input E.
7	NC	No connect.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No connect.
11	V_{OE}	Logic Output E.
12	V_{OD}	Logic Output D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

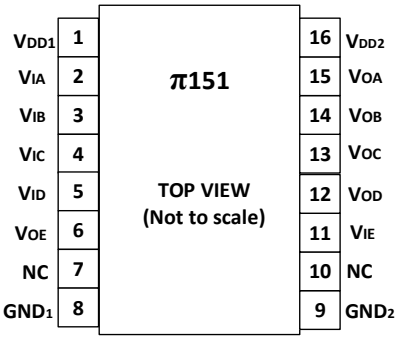


Figure5. π151 Pin Configuration

π151 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{ID}	Logic Input D.
6	V_{OE}	Logic Output E.
7	NC	No connect.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No connect.
11	V_{IE}	Logic Input E.
12	V_{OD}	Logic Output D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

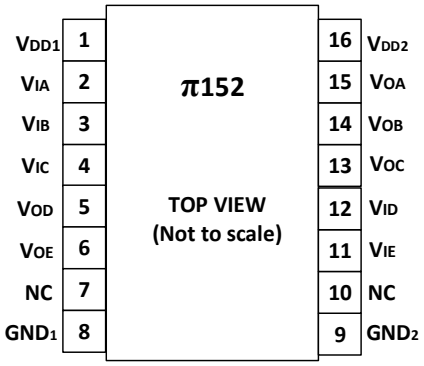


Figure6. π152 Pin Configuration

π152 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	V_{IC}	Logic Input C.
5	V_{OD}	Logic Output D.
6	V_{OE}	Logic Output E.
7	NC	No connect.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No connect.
11	V_{IE}	Logic Input E.
12	V_{ID}	Logic Input D.
13	V_{OC}	Logic Output C.
14	V_{OB}	Logic Output B.
15	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2.

APPLICATIONS INFORMATION

OVERVIEW

The π150/π151/π152 transmit data across an isolation barrier by layers of silicon oxide isolation.

The π150/π151/π152 have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V, and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or the fail-safe output state of high.

PCB LAYOUT

The π150/π151/π152 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 7). Bypass capacitors are most conveniently connected between Pin 1 and Pin 4 for V_{DD1} and between Pin 5 and Pin 8 for V_{DD2}. The recommended bypass capacitor value is between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 10 mm.

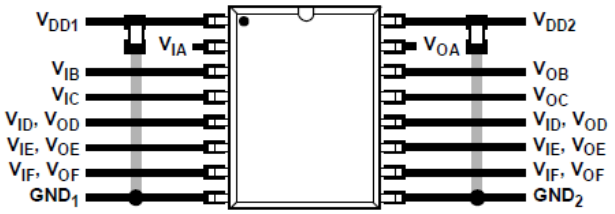


Figure7.Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, ensure that board coupling across the isolation barrier is minimized. Furthermore, design the board layout such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the Absolute Maximum Ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a Logic 0 output may differ from the propagation delay to a Logic 1 output.

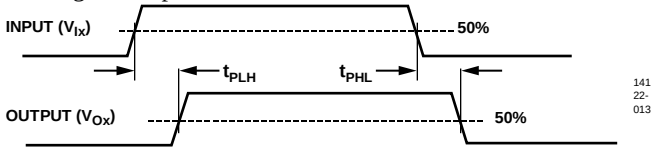


Figure 8. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel matching is the maximum amount the propagation delay differs between channels within a single π150/π151/π152 component.

Propagation delay skew is the maximum amount the propagation delay differs between multiple π150/π151/π152 components operating under the same conditions.

JITTER MEASUREMENT

Figure 9 shows the eye diagram for the π150/π151/π152. The measurement was taken using an Keysight 81160A pulse pattern generator at 10 Mbps with pseudorandom bit sequences (PRBS) 2(n − 1), n = 14, for 5 V supplies. Jitter was measured with the Keysight DSOS104A oscilloscope, 1 GHz, 20 GS/s with the DPOJET jitter and eye diagram analysis tools. The result shows a typical measurement on the π150/π151/π152 with 47 ps p-p jitter.

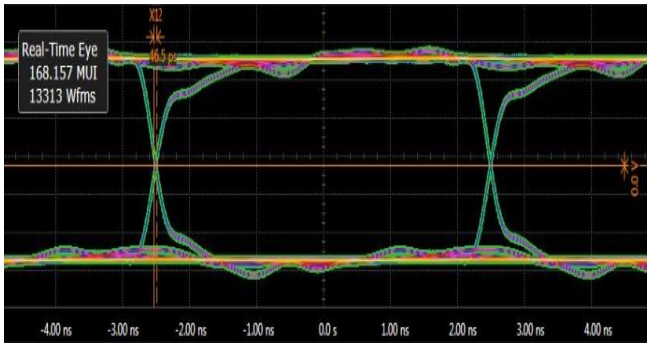


Figure9. π150/π151/π152 Eye Diagram

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components that allows the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and, therefore, can provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material

group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. The material group and creepage for the π150/π151/π152 isolators are presented in Table 5.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by its thickness, material properties, and the voltage stress applied. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. It is the working voltage applicable to tracking that is specified in most standards.

Testing and modeling show that the primary driver of long term degradation is displacement current in the silicon oxide insulation causing incremental damage. The stress on the insulation can be broken down into broad categories, such as dc stress, which causes very little wear out because there is no displacement current, and an ac component time varying voltage stress, which causes wear out.

The ratings in certification documents are usually based on 60 Hz sinusoidal stress because this reflects isolation from line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as is shown in Equation 2. For insulation wear out with the silicon oxide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:

V_{RMS} is the total rms working voltage.

$V_{AC\ RMS}$ is the time varying portion of the working voltage.

V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 $V_{AC\ RMS}$ and a 400 V_{DC} bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 10 and the following equations.

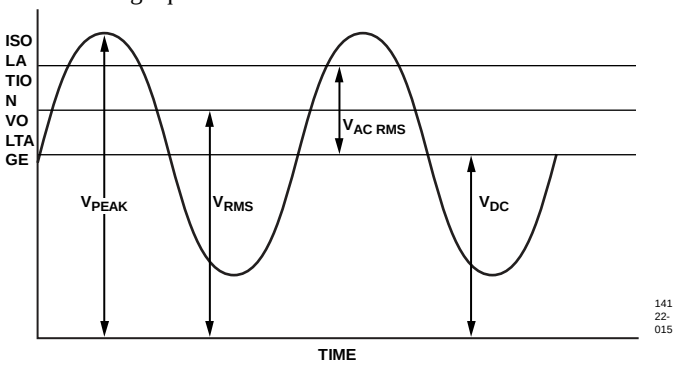


Figure10. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\ RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

$$V_{RMS} = 466\ \text{V}$$

This is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\ RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

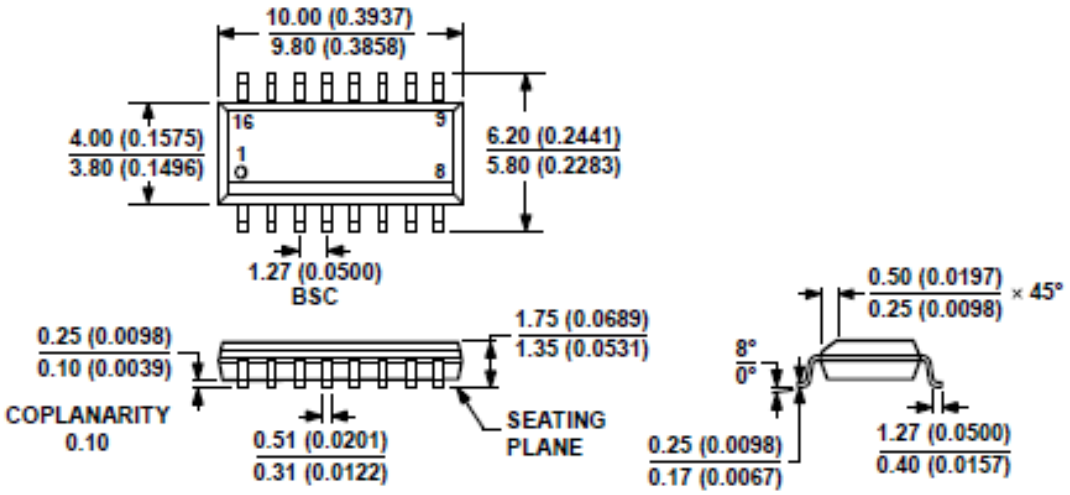
$$V_{AC\ RMS} = \sqrt{466^2 - 400^2}$$

$$V_{AC\ RMS} = 240\ \text{V rms}$$

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is not sinusoidal. The value is compared to the limits for working voltage in Table 10 for the expected lifetime, less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit in Table 10 is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

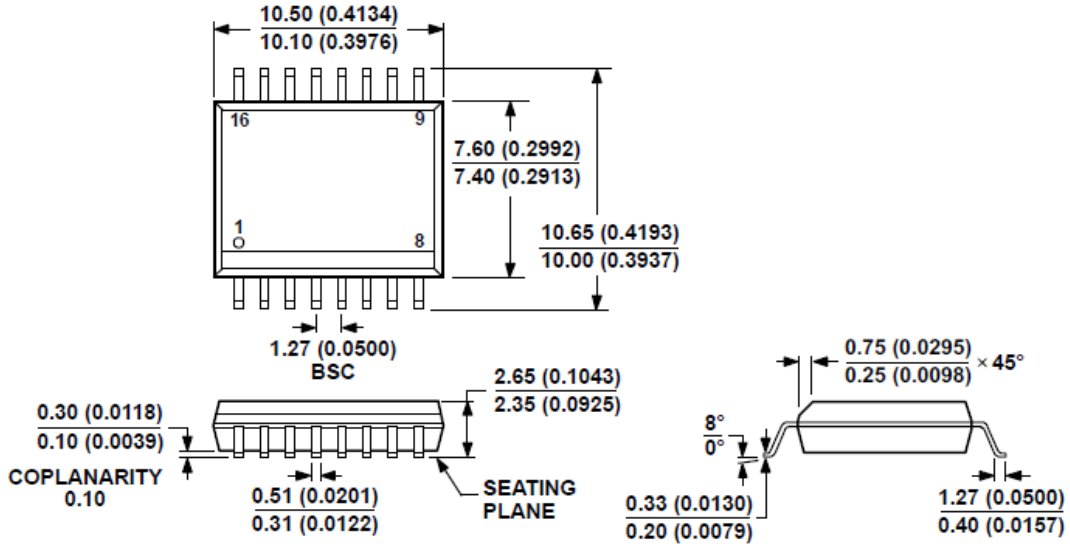
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AC

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure11. 16-Lead Standard Small Outline Package [SOIC_N]
N/Arrow Body (S-16-N)
Dimensions shown in millimeters and (inches)

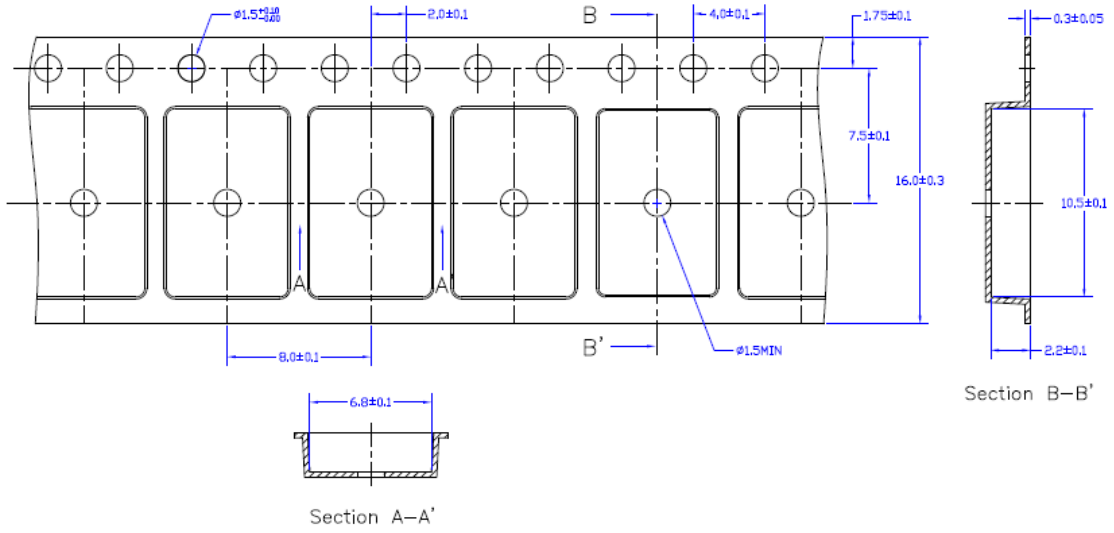


COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure12. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body (S-16-W)
Dimensions shown in millimeters and (inches)

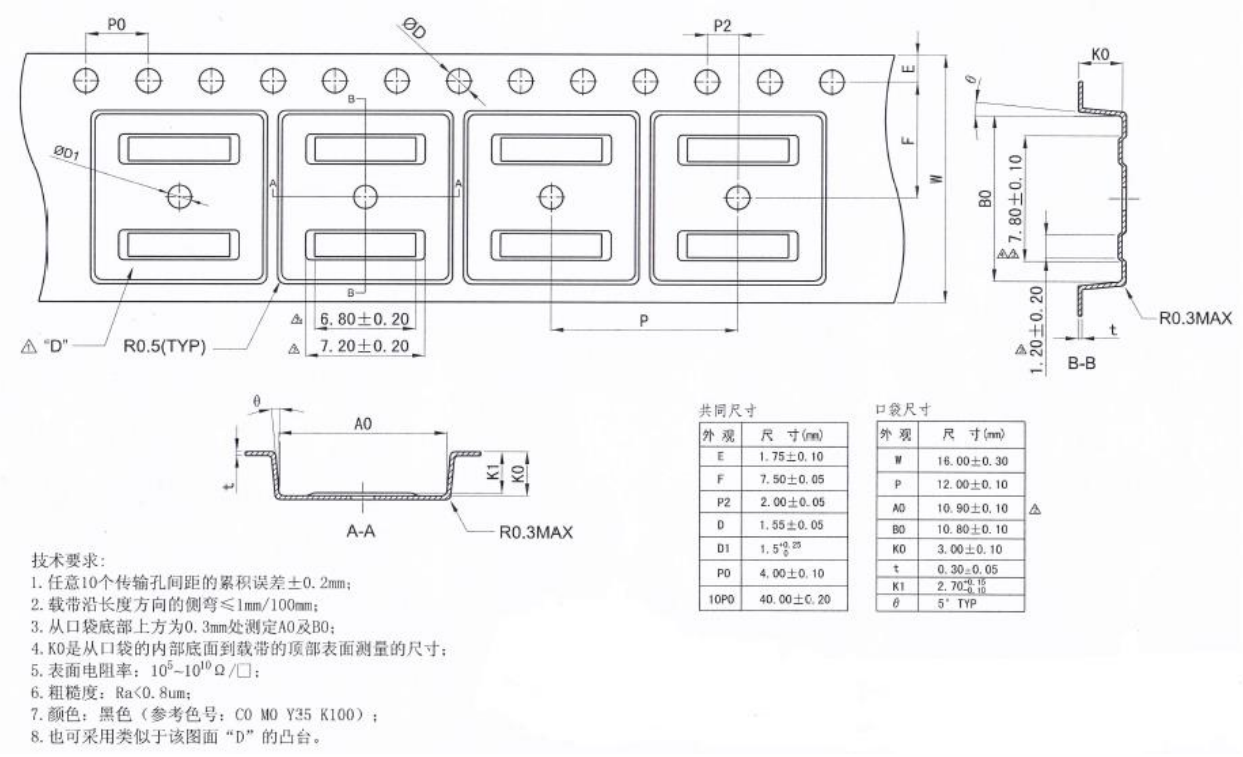
REEL INFORMATION

S-16-N



NOTES:
1.10 procket hole pitch cumulative tolerance ±0.2
2.Carrier camber is within 1mm in 100mm
3.MATERIAL:PS Black Tape
4.ALL DIMS IN MM
5.There must not be foreign body adhesion and the state of the surface must be excellent
6.22"Reel, 48125 pockets (385m)
7.Surface resistance 1X10E5≤Rs≤1X10E9 OHMS/SQ

S-16-W



技术要求：
1. 任意10个传输孔间距的累积误差±0.2mm；
2. 载带沿长度方向的侧弯≤1mm/100mm；
3. 从口袋底部上方为0.3mm处测定A0及B0；
4. K0是从口袋的内部底面到载带的顶部表面测量的尺寸；
5. 表面电阻率：10^5~10^{10}Ω/□；
6. 粗糙度：Ra<0.8um；
7. 颜色：黑色（参考色号：C0 M0 Y35 K100）；
8. 也可采用类似于该图面"D"的凸台。

共同尺寸

外观	尺寸(mm)
E	1.75±0.10
F	7.50±0.05
P2	2.00±0.05
D	1.55±0.05
D1	1.5 +0.25 0
P0	4.00±0.10
10P0	40.00±0.20

口袋尺寸

外观	尺寸(mm)
W	16.00±0.30
P	12.00±0.10
A0	10.90±0.10 △
B0	10.80±0.10
K0	3.00±0.10
t	0.30±0.05
K1	2.70 +0.15 −0.10
θ	5° TYP

ORDERING GUIDE

Model	Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	Package Option	Quantity
π150A41	−40°C to +125°C	5	0	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π150A40	−40°C to +125°C	5	0	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π151A41	−40°C to +125°C	4	1	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π151A40	−40°C to +125°C	4	1	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π152A41	−40°C to +125°C	3	2	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π152A40	−40°C to +125°C	3	2	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π150M41	−40°C to +125°C	5	0	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π150M40	−40°C to +125°C	5	0	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π151M41	−40°C to +125°C	4	1	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π151M40	−40°C to +125°C	4	1	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π152M41	−40°C to +125°C	3	2	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π152M40	−40°C to +125°C	3	2	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π150U41	−40°C to +125°C	5	0	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π150U40	−40°C to +125°C	5	0	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π151U41	−40°C to +125°C	4	1	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π151U40	−40°C to +125°C	4	1	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π152U41	−40°C to +125°C	3	2	4	High	16-Lead SOIC_N	S-16-N	4000 per reel
π152U40	−40°C to +125°C	3	2	4	Low	16-Lead SOIC_N	S-16-N	4000 per reel
π150A61	−40°C to +125°C	5	0	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π150A60	−40°C to +125°C	5	0	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π151A61	−40°C to +125°C	4	1	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π151A60	−40°C to +125°C	4	1	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π152A61	−40°C to +125°C	3	2	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π152A60	−40°C to +125°C	3	2	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π150M61	−40°C to +125°C	5	0	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π150M60	−40°C to +125°C	5	0	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π151M61	−40°C to +125°C	4	1	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π151M60	−40°C to +125°C	4	1	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π152M61	−40°C to +125°C	3	2	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π152M60	−40°C to +125°C	3	2	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π150U61	−40°C to +125°C	5	0	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π150U60	−40°C to +125°C	5	0	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π151U61	−40°C to +125°C	4	1	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π151U60	−40°C to +125°C	4	1	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel
π152U61	−40°C to +125°C	3	2	6	High	16-Lead SOIC_W	S-16-W	1500 per reel
π152U60	−40°C to +125°C	3	2	6	Low	16-Lead SOIC_W	S-16-W	1500 per reel

Part number named rule: