2Pai Semi

Enhanced ESD, 3.0 kV rms/6.0 kV rms 600Mbps Dual-Channel Digital Isolators

Data Sheet **π120A/π121A/π122A**

FEATURES

- **Ultra low power consumption:**
  - **0.35mA/Channel**
- **High data rate:** **π12xAxx: 600Mbps**
  - **π12xExx: 200Mbps**
  - **π12xMxx: 10Mbps**
  - **π12xUxx: 150kbps**
- **High common-mode transient immunity: 50 kV/μs typical**
- **High robustness to radiated and conducted noise**
- **Low propagation delay:**
  - **5 ns typical for 5 V operation**
  - **7 ns typical for 3.3 V operation**
- **Isolation voltages:**
  - **π12xx3x: AC 3000Vrms**
  - **π12xx6x: AC 6000Vrms**
- **High ESD rating:**
  - **ESDA/JEDEC JS-001-2017**
  - **Human body model (HBM) ±7kV, all pins**
- **Safety and regulatory approvals：**
  - **UL certificate number: E494497**
    - **3000Vrms/6000Vrms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice 5A(Pending)**
  - **VDE certificate number: 40047929**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 565V peak/849V peak**
  - **CQC certification per GB4943.1-2011(Pending)**
- **3 V to 5.5 V level translation**
- **Wide temperature range: -40°C to 125°C**
- **8/16-lead, RoHS-compliant, (W)SOIC package**

APPLICATIONS

- **General-purpose multichannel isolation**
- **Industrial field bus isolation**

GENERAL DESCRIPTION

The π1xxxxx are 2PaiSemi digital isolators product family. By using maturated standard semiconductor CMOS technology and innovative design, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 3.0 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier.

The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

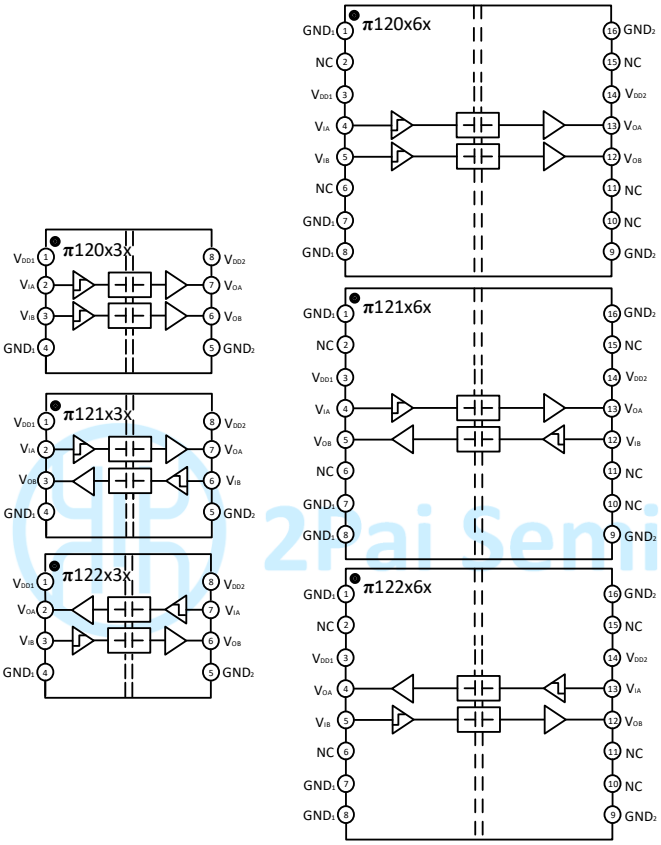

Figure1. π120xxx/π121xxx/π122xxx functional Block Diagram

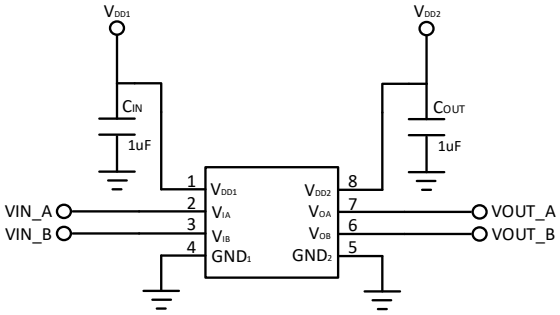

Figure2. π120xxx Typical Application Circuit

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http://www.rpsemi.com/

PIN CONFIGURATIONS AND FUNCTIONS

π120A3x Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

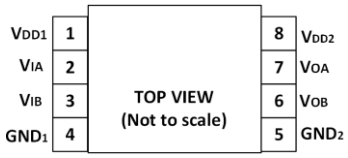


Figure3. π120A3x Pin Configuration

π121A3x Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{IA}	Logic Input A.
3	V_{OB}	Logic Output B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{IB}	Logic Input B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

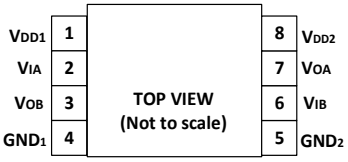


Figure4. π121A3x Pin Configuration

π122A3x Pin Function Descriptions

Pin No.	Name	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1.
2	V_{OA}	Logic Output A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
5	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{IA}	Logic Input A.
8	V_{DD2}	Supply Voltage for Isolator Side 2.

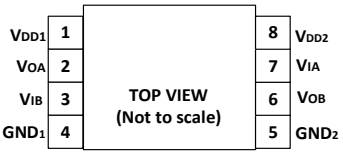


Figure5. π122A3x Pin Configuration

π120A6x Pin Function Descriptions

Pin No.	Name	Description
1	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{IA}	Logic Input A.
5	V_{IB}	Logic Input B.
6	NC	No Connect.
7	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

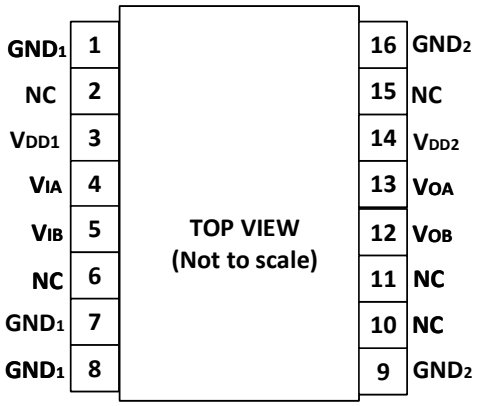


Figure6. π120A6x Pin Configuration

10	NC	No Connect.
11	NC	No Connect.
12	V_{OB}	Logic Output B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

π121A6x Pin Function Descriptions

Pin No.	Name	Description
1	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{IA}	Logic Input A.
5	V_{OB}	Logic Output B.
6	NC	No Connect.
7	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{IB}	Logic Input B.
13	V_{OA}	Logic Output A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

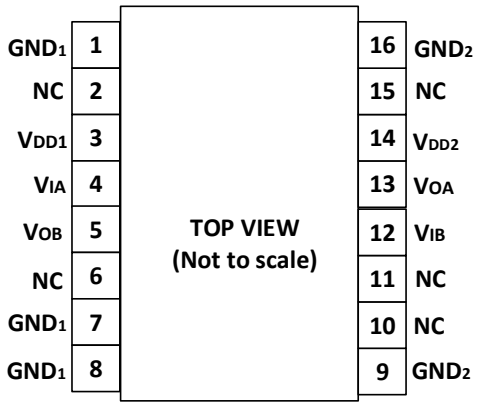


Figure7. π121A6x Pin Configuration

π122A6x Pin Function Descriptions

Pin No.	Name	Description
1	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
2	NC	No Connect.
3	V_{DD1}	Supply Voltage for Isolator Side 1.
4	V_{OA}	Logic Output A.
5	V_{IB}	Logic Input B.
6	NC	No Connect.
7	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
8	GND_1	Ground 1. This pin is the ground reference for Isolator Side 1.
9	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.
10	NC	No Connect.
11	NC	No Connect.
12	V_{OB}	Logic Output B.
13	V_{IA}	Logic Input A.
14	V_{DD2}	Supply Voltage for Isolator Side 2.
15	NC	No Connect.
16	GND_2	Ground 2. This pin is the ground reference for Isolator Side 2.

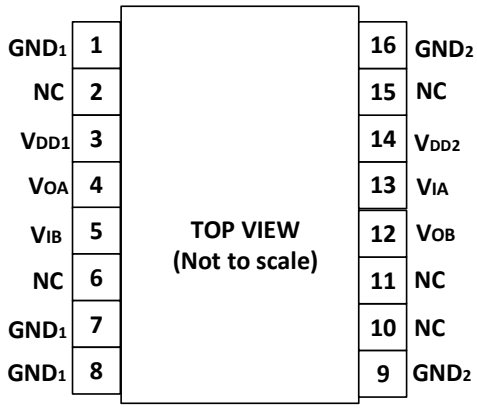


Figure8. π122A6x Pin Configuration

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 1. Absolute Maximum Ratings[4]

Parameter	Rating
Supply Voltages (V_{DD1}-GND_1, V_{DD2}-GND_2)	−0.5 V to +7.0 V
Input Voltages (V_{IA}, V_{IB})[1]	−0.5 V to V_{DDx} + 0.5 V
Output Voltages (V_{OA}, V_{OB})[1]	−0.5 V to V_{DDx} + 0.5 V
Average Output Current per Pin[2] Side 1 Output Current (I_{O1})	−10 mA to +10 mA
Average Output Current per Pin[2] Side 2 Output Current (I_{O2})	−10 mA to +10 mA
Common-Mode Transients Immunity[3]	−150 kV/µs to +150 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.
[2] See Figure9 for the maximum rated current values for various temperatures.
[3] See Figure14 for Common-mode transient immunity (CMTI) measurement.
[4] Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DDx} [1]	3		5.5	V
High Level Input Signal Voltage	V_{IH}	0.7*V_{DDx}[1]		V_{DDx}[1]	V
Low Level Input Signal Voltage	V_{IL}	0		0.3*V_{DDx}[1]	V
High Level Output Current	I_{OH}	-6			mA
Low Level Output Current	I_{OL}			6	mA
Maximum Data Rate		0		600	Mbps
Junction Temperature	T_J	-40		150	°C
Ambient Operating Temperature	T_A	-40		125	°C

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Truth Tables

Table 3. π120xxx/π121xxx/π122xxx Truth Table

V_{Ix} Input[1]	V_{DDI} State[1]	V_{DDO} State[1]	Default Low V_{Ox} Output[1]	Default High V_{Ox} Output[1]	Test Conditions /Comments
Low	Powered[2]	Powered[2]	Low	Low	Normal operation
High	Powered[2]	Powered[2]	High	High	Normal operation
Open	Powered[2]	Powered[2]	Low	High	Default output
Don't Care[4]	Unpowered[3]	Powered[2]	Low	High	Default output[5]
Don't Care[4]	Powered[2]	Unpowered[3]	High Impedance	High Impedance	

Notes:
[1] V_{Ix}/V_{Ox} are the input/output signals of a given channel (A or B). V_{DDI}/V_{DDO} are the supply voltages on the input/output signal sides of this given channel.
[2] Powered means V_{DDx}≥ 2.9 V
[3] Unpowered means V_{DDx} < 2.3V

[4] Input signal (V_{Ix}) must be in a low state to avoid powering the given V_{DDI}[1] through its ESD protection circuitry.

[5] If the V_{DDI} goes into unpowered status, the channel outputs the default logic signal after around 1us. If the V_{DDI} goes into powered status, the channel outputs the input status logic signal after around 1us.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 4. Switching Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Minimum Pulse Width	PW			1.6	ns	Within pulse width distortion (PWD) limit
Maximum Data Rate		600			Mbps	Within PWD limit
Propagation Delay Time[1,4]	t_{pHL}, t_{pLH}	3.5	5.0	7.5	ns	The different time between 50% input signal to 50% output signal 50% @ 5V_{DC} supply
		5.5	7.0	9.5	ns	@ 3.3V_{DC} supply
Pulse Width Distortion[4]	PWD	0	0.3	0.8	ns	The max different time between t_{pHL} and t_{pLH}@ 5V_{DC} supply. And The value is | t_{pHL} - t_{pLH} |
		0	0.3	0.8	ns	@ 3.3V_{DC} supply
Part to Part Propagation Delay Skew[4]	t_{PSK}			1	ns	The max different propagation delay time between any two devices at the same temperature, load and voltage @ 5V_{DC} supply
				1	ns	@ 3.3V_{DC} supply
Channel to Channel Propagation Delay Skew[4]	t_{CSK}		0	1	ns	The max amount propagation delay time differs between any two output channels in the single device @ 5V_{DC} supply.
			0	0.8	ns	@ 3.3V_{DC} supply
Output Signal Rise/Fall Time[4]	t_r/t_f		0.7		ns	10% to 90% signal terminated 50Ω, See Figure10.
Dynamic Input Supply Current per Channel	$I_{DDI (D)}$		6.8		μA /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V_{DC} Supply
Dynamic Output Supply Current per Channel	$I_{DDO (D)}$		40.5		μA /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 5V_{DC} Supply
Dynamic Input Supply Current per Channel	$I_{DDI (D)}$		4.3		μA /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V_{DC} Supply
Dynamic Output Supply Current per Channel	$I_{DDO (D)}$		26.0		μA /Mbps	Inputs switching, 50% duty cycle square wave, CL = 0 pF @ 3.3V_{DC} Supply
Common-Mode Transient Immunity[3]	CMTI		50		kV/μs	V_{IN} = V_{DDx}[2] or 0V, V_{CM} = 1000 V.
Jitter			90		ps p-p	See the Jitter Measurement section
			15		ps rms	See the Jitter Measurement section
ESD（HBM - Human body model）	ESD		±7		kV	all pins

Notes:

[1] t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See figure 16.

[2] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

[3] See Figure14 for Common-mode transient immunity (CMTI) measurement.

[4] Output Signal Terminated 50Ω.

Table 5. DC Specifications

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
High Level Input Signal Voltage	V_{IH}			0.7*V_{DDx}[1]	V	
Low Level Input Signal Voltage	V_{IL}	0.3* V_{DDX}[1]			V	
High Level Output Voltage	V_{OH} [1]	V_{DDx} – 0.1	V_{DDx}		V	−20 µA output signal
		V_{DDx} – 0.2	V_{DDx} – 0.1		V	−2 mA output signal
Low Level Output Voltage	V_{OL}		0	0.1	V	20 µA output signal
			0.1	0.2	V	2 mA output signal
Input Current per Signal Channel	I_{IN}	−10	0.5	10	µA	0 V ≤ Signal voltage ≤ V_{DDX}[1]
V_{DDx}[1] Undervoltage Rising Threshold	V_{DDxUV+}	2.45	2.65	2.9	V	
V_{DDx}[1] Undervoltage Falling Threshold	V_{DDxUV-}	2.3	2.5	2.75	V	
V_{DDx}[1] Hysteresis	V_{DDxUVH}		0.15		V	

Notes:
[1] V_{DDx} is the side voltage power supply V_{DD}, where x = 1 or 2.

Table 6. Quiescent Supply Current

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
π120Axx Quiescent Supply Current @ 5V_{DC} Supply	$I_{DD1 (Q)}$	101	126	164	µA	0V Input signal
	$I_{DD2 (Q)}$	448	560	728	µA	0V Input signal
	$I_{DD1 (Q)}$	102	128	166	µA	5V Input signal
	$I_{DD2 (Q)}$	410	512	666	µA	5V Input signal
@ 3.3V_{DC} Supply	$I_{DD1 (Q)}$	72	90	117	µA	0V Input signal
	$I_{DD2 (Q)}$	482	602	783	µA	0V Input signal
	$I_{DD1 (Q)}$	74	92	120	µA	3.3V Input signal
	$I_{DD2 (Q)}$	446	558	725	µA	3.3V Input signal
π121Axx Quiescent Supply Current @ 5V_{DC} Supply	$I_{DD1 (Q)}$	274	343	446	µA	0V Input signal
	$I_{DD2 (Q)}$	274	343	446	µA	0V Input signal
	$I_{DD1 (Q)}$	256	320	416	µA	5V Input signal
	$I_{DD2 (Q)}$	256	320	416	µA	5V Input signal
@ 3.3V_{DC} Supply	$I_{DD1 (Q)}$	277	346	450	µA	0V Input signal
	$I_{DD2 (Q)}$	277	346	450	µA	0V Input signal
	$I_{DD1 (Q)}$	260	325	423	µA	3.3V Input signal
	$I_{DD2 (Q)}$	260	325	423	µA	3.3V Input signal
π122Axx Quiescent Supply Current @ 5V_{DC} Supply	$I_{DD1 (Q)}$	274	343	446	µA	0V Input signal
	$I_{DD2 (Q)}$	274	343	446	µA	0V Input signal
	$I_{DD1 (Q)}$	256	320	416	µA	5V Input signal
	$I_{DD2 (Q)}$	256	320	416	µA	5V Input signal
@ 3.3V_{DC} Supply	$I_{DD1 (Q)}$	277	346	450	µA	0V Input signal
	$I_{DD2 (Q)}$	277	346	450	µA	0V Input signal
	$I_{DD1 (Q)}$	260	325	423	µA	3.3V Input signal
	$I_{DD2 (Q)}$	260	325	423	µA	3.3V Input signal

Table 7. Total Supply Current vs. Data Throughput (C_L = 0 pF)

V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC}±10% or 5V_{DC}±10%, T_A=25°C, C_L = 0 pF, unless otherwise noted.

Parameter	Symbol	150 Kbps			10 Mbps			100 Mbps			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
π120Axx Supply Current @ 5V_{DC}	I_{DD1}		0.13	0.20		0.28	0.42		2.12	3.18	mA
	I_{DD2}		0.54	0.81		1.31	1.96		7.84	11.77	mA
@ 3.3V_{DC}	I_{DD1}		0.09	0.14		0.19	0.28		1.48	2.23	mA
	I_{DD2}		0.58	0.87		1.08	1.625		5.07	7.61	mA
π121Axx Supply Current @ 5V_{DC}	I_{DD1}		0.34	0.50		0.79	1.19		4.98	7.47	mA
	I_{DD2}		0.34	0.50		0.79	1.19		4.98	7.47	mA
@ 3.3V_{DC}	I_{DD1}		0.34	0.50		0.64	0.95		3.28	4.92	mA
	I_{DD2}		0.34	0.50		0.64	0.95		3.28	4.92	mA
π122Axx Supply Current @ 5V_{DC}	I_{DD1}		0.34	0.50		0.79	1.19		4.98	7.47	mA
	I_{DD2}		0.34	0.50		0.79	1.19		4.98	7.47	mA
@ 3.3V_{DC}	I_{DD1}		0.34	0.50		0.64	0.95		3.28	4.92	mA
	I_{DD2}		0.34	0.50		0.64	0.95		3.28	4.92	mA

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 8. Insulation Specifications

Parameter	Symbol	Value		Unit	Test Conditions/Comments
		π12xA3x	π12xA6x		
Rated Dielectric Insulation Voltage		3000	6000	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L (CLR)	4	**	mm min	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L (CRP)	4	**	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	4.5	**	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		8	**	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	**	V	DIN IEC 112/VDE 0303 Part 1
Material Group		II	**		Material Group (DIN VDE 0110, 1/89, Table 1)

PACKAGE CHARACTERISTICS

Table 9. Package Characteristics

Parameter	Symbol	Typical Value		Unit	Test Conditions/Comments
		π12xA3x	π12xA6x		
Resistance (Input to Output)[1]	R_{I-O}	10^{11}	10^{11}	Ω	
Capacitance (Input to Output)[1]	C_{I-O}	0.6	0.6	pF	@1MHz
Input Capacitance[2]	C_I	3	3	pF	@1MHz
IC Junction to Ambient Thermal Resistance	θ_{JA}	100	45	°C/W	Thermocouple located at center of package underside

Notes:

[1]The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4(WSOIC-16 Pin 1-Pin8) are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8(WSOIC-16 Pin 9-Pin16) are shorted together as the other terminal.

[2]Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table10. Regulatory

Regulatory	π12xA3x	π12xA6x
UL	Recognized under UL 1577 Component Recognition Program[1] Single Protection, 3000 V rms Isolation Voltage File (E494497)	Recognized under UL 1577 Component Recognition Program[1] Single Protection, *** V rms Isolation Voltage File (pending)
CSA	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 400 V rms (565 V peak) Reinforced insulation at 200 V rms (283 V peak) File (pending)	Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at *** V rms (**** V peak) Reinforced insulation at *** V rms (*** V peak) File (pending)
VDE	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2] Basic insulation, V_{IORM} = 565 V peak, V_{IOSM} = 4615 V peak File (40047929)	DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2] Basic insulation, V_{IORM} = *** V peak, V_{IOSM} = **** V peak Reinforced insulation, V_{IORM} =*** V peak, V_{IOSM} = 10 kV peak File (pending)
CQC	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 400 V rms (565 V peak) working voltage Reinforced insulation at 200 V rms (283 V peak) File (pending)	Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at *** V rms (*** V peak) working voltage Reinforced insulation at *** V rms (*** V peak) File (pending)

Notes:

[1] In accordance with UL 1577, each π120A3x/π121A3x/π122A3x is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec; each π120A6x/π121A6x/π122A6x is proof tested by applying an isulation test voltage ≥ 7200 V rms for 1 sec

[2] In accordance with DIN V VDE V 0884-10, each π120A3x/π121A3x/π122A3x is proof tested by applying an insulation test voltage ≥ 1059 V peak for 1 sec (partial discharge detection limit = 5 pC); each π120A6x/π121A6x/π122A6x is proof tested by ≥ *** V peak for 1 sec. The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 11. VDE Insulation Characteristics

Description	Test Conditions/Comments	Symbol	Characteristic		Unit
			π12xx3x	π12xx6x	
Installation Classification per DIN VDE 0110					
For Rated Mains Voltage ⩽ 150 V rms			I to IV	***	
For Rated Mains Voltage ≤ 300 V rms			I to III	***	
For Rated Mains Voltage ≤ 400 V rms			I to III	***	

Climatic Classification			40/105/21	***	
Pollution Degree per DIN VDE 0110, Table 1			2	*	
Maximum Working Insulation Voltage		V_{IORM}	565	***	V peak
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd\,(m)}$, 100% production test, tini = t_m = 1 sec, partial discharge < 5 pC	$V_{pd\,(m)}$	1059	***	V peak
Input to Output Test Voltage, Method A					
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC	$V_{pd\,(m)}$	848	***	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd\,(m)}$, t_{ini} = 60 sec, t_m = 10 sec, partial discharge < 5 pC		678	***	V peak
Highest Allowable Overvoltage		V_{IOTM}	4200	***	V peak
Surge Isolation Voltage Basic	Basic insulation, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4615	***	V peak
Surge Isolation Voltage Reinforced	Reinforced insulation, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}		***	V peak
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)				
Maximum Junction Temperature		T_S	150	***	°C
Total Power Dissipation at 25°C		P_S	1.56	***	W
Insulation Resistance at T_S	V_{IO} = 800 V	R_S	>10^9	***	Ω

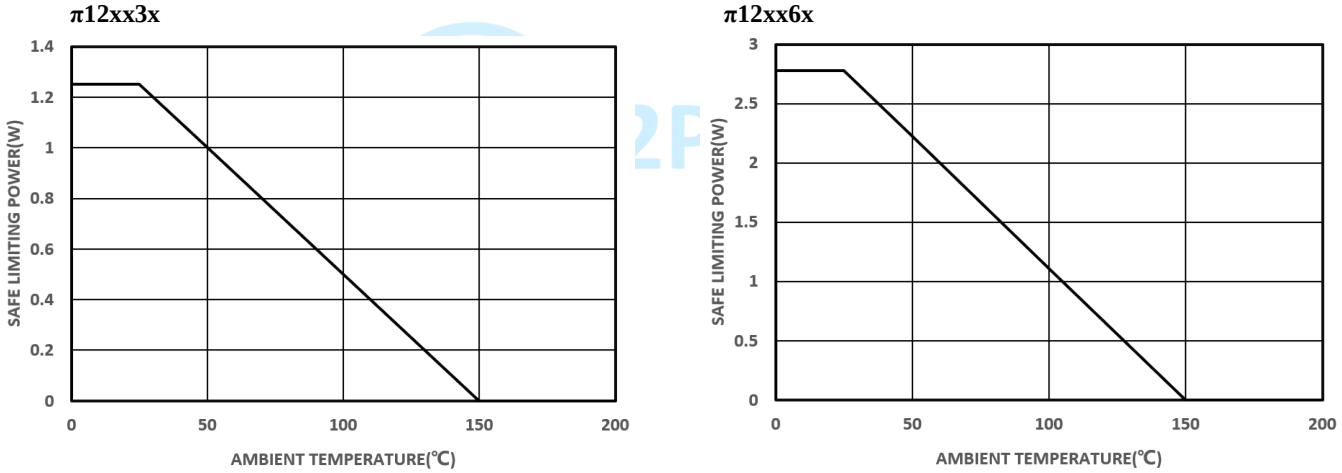


Figure9. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE

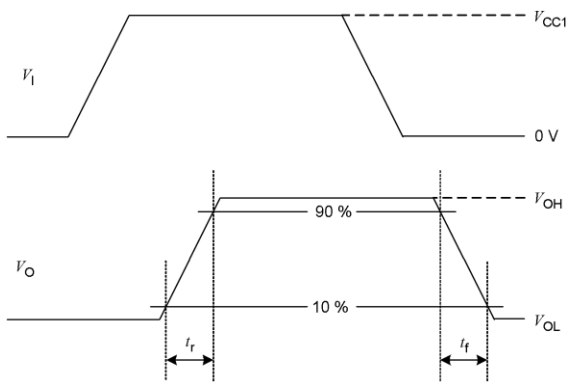


Figure10. Transition time waveform measurement

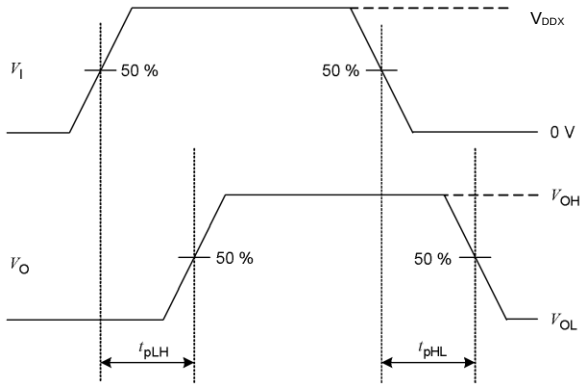


Figure11. Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The π1xxxxx are 2PaiSemi digital isolators product family. By using maturated standard semiconductor CMOS technology and innovative design, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices and other integrated isolators. The π1xxxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 3.0 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The π120Axx/π121Axx/π122Axx are the outstanding 600 Mbps dual-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic.

The π120Axx/π121Axx/π122Axx have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2. The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μF and 10 μF.

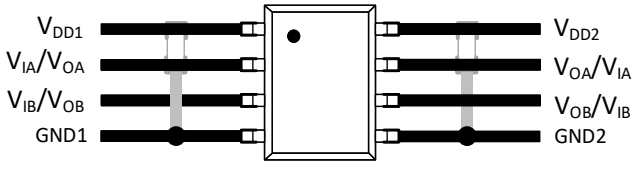


Figure12.Recommended Printed Circuit Board Layout

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

JITTER MEASUREMENT

The eye diagram shown in the Figure13 provides the jitter measurement result for the π120Axx/π121Axx/π122Axx. The Keysight 81160A pulse function arbitrary generator works as the data source for the π120Axx/π121Axx/π122Axx, which generates 100Mbps pseudo random bit sequence（PRBS）. The Keysight DSOS104A digital storage oscilloscope captures the π120Axx/π121Axx/π122Axx output waveform and recoveries the eye diagram with the SDA jitter tools and eye diagram analysis tools. The result shows a typical measurement 90ps p-p jitter.

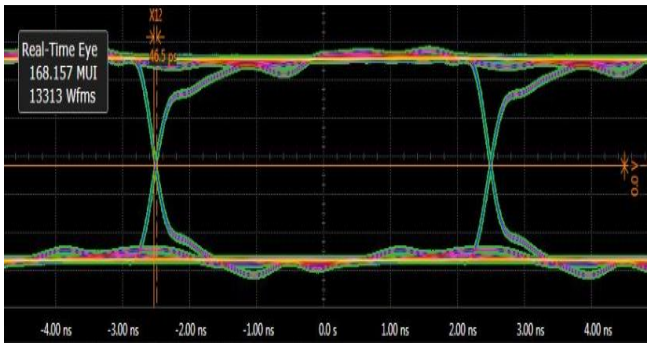


Figure13. π120Axx/π121Axx/π122Axx Eye Diagram

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of π1xxxxx isolator under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, The common-mode pulse generator (G_1) will be capable of providing fast rising and falling pulses of specified magnitude and duration

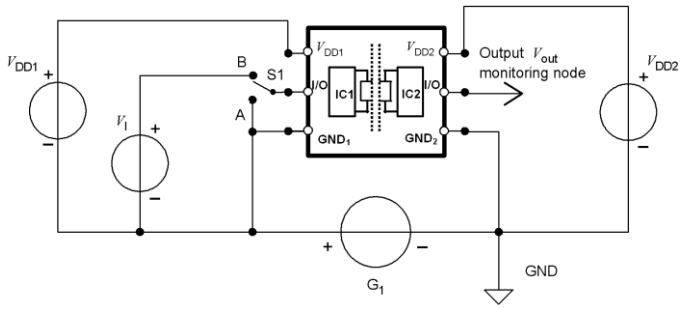


Figure14. Common-mode transient immunity (CMTI) measurement

of the common-mode pulse (V_{CM}) and the maximum common-mode slew rates (dV_{CM}/dt) can be applied to π1xxxxx isolator coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π1xxxxx isolator and shall be capable of providing positive transients as well as negative transients.

OUTLINE DIMENSIONS

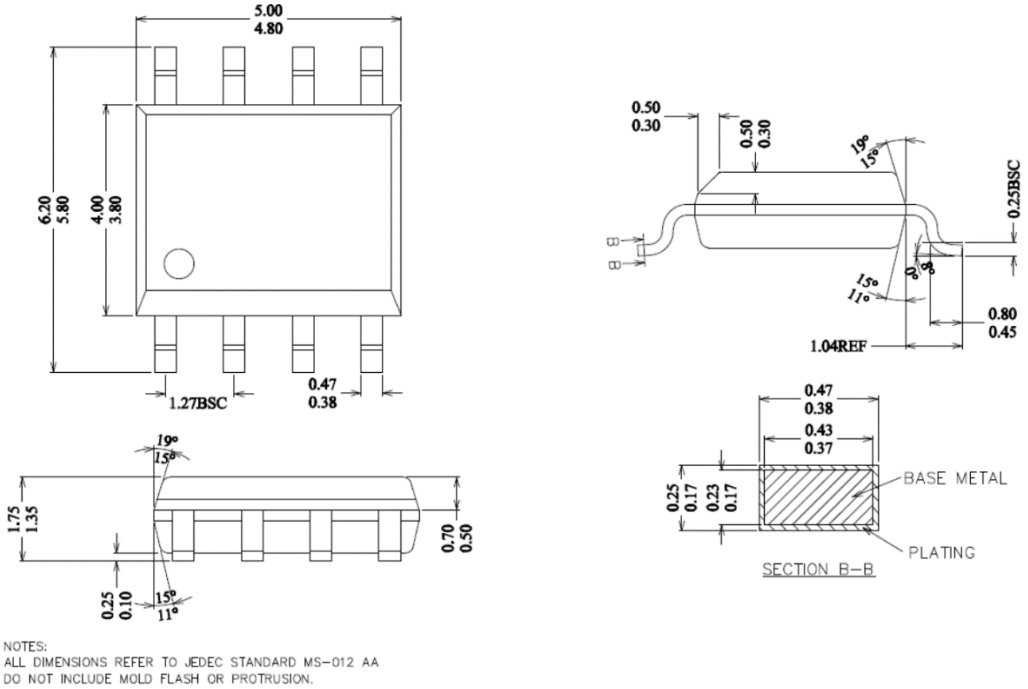


Figure15. 8-Lead Standard Small Outline Package [8-Lead SOIC_N]

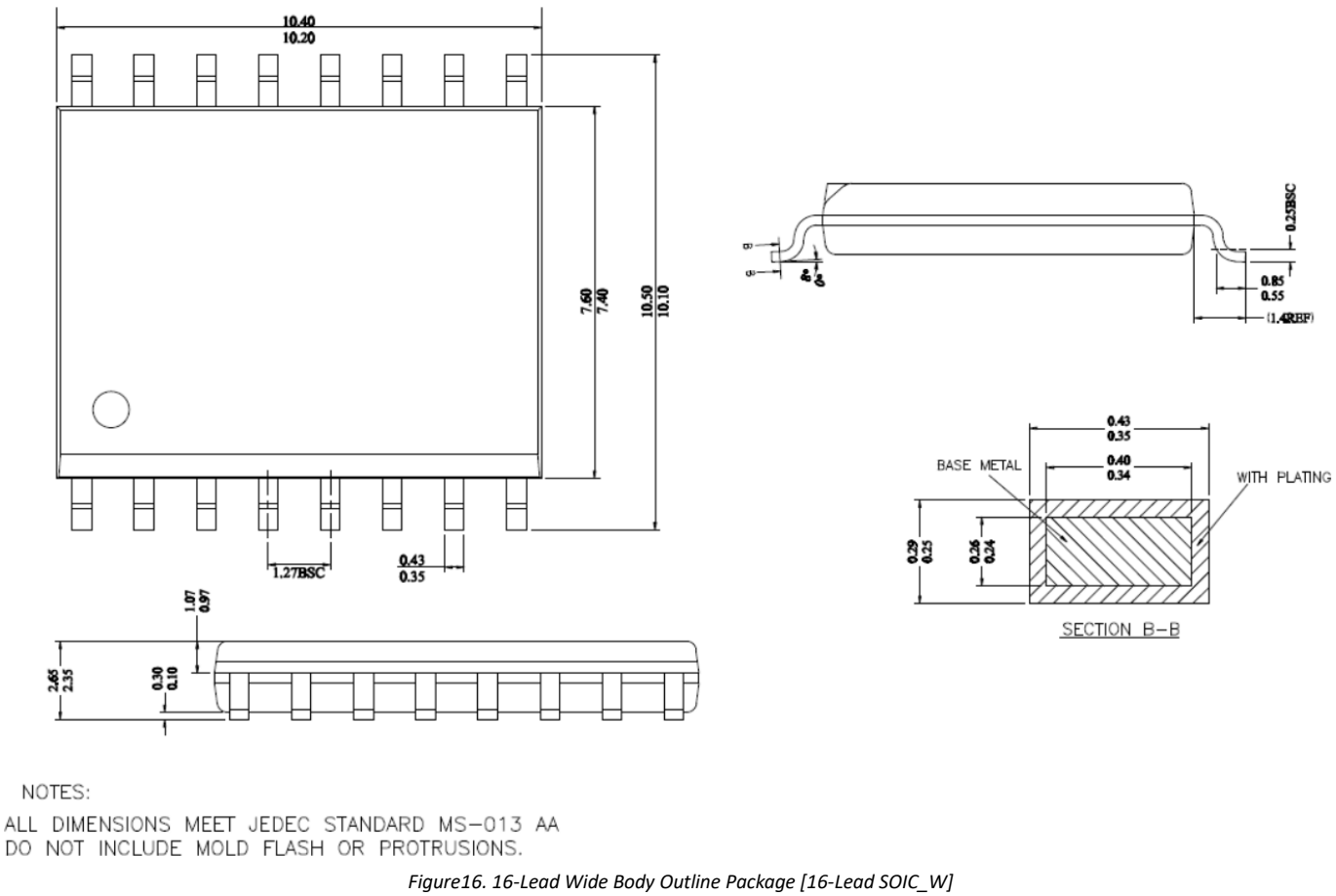
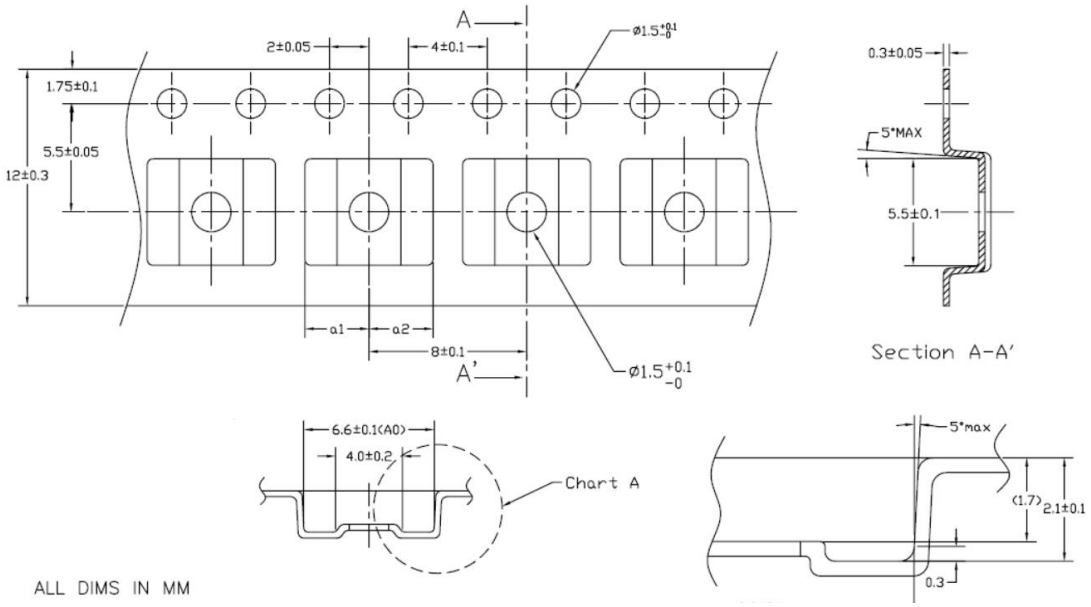


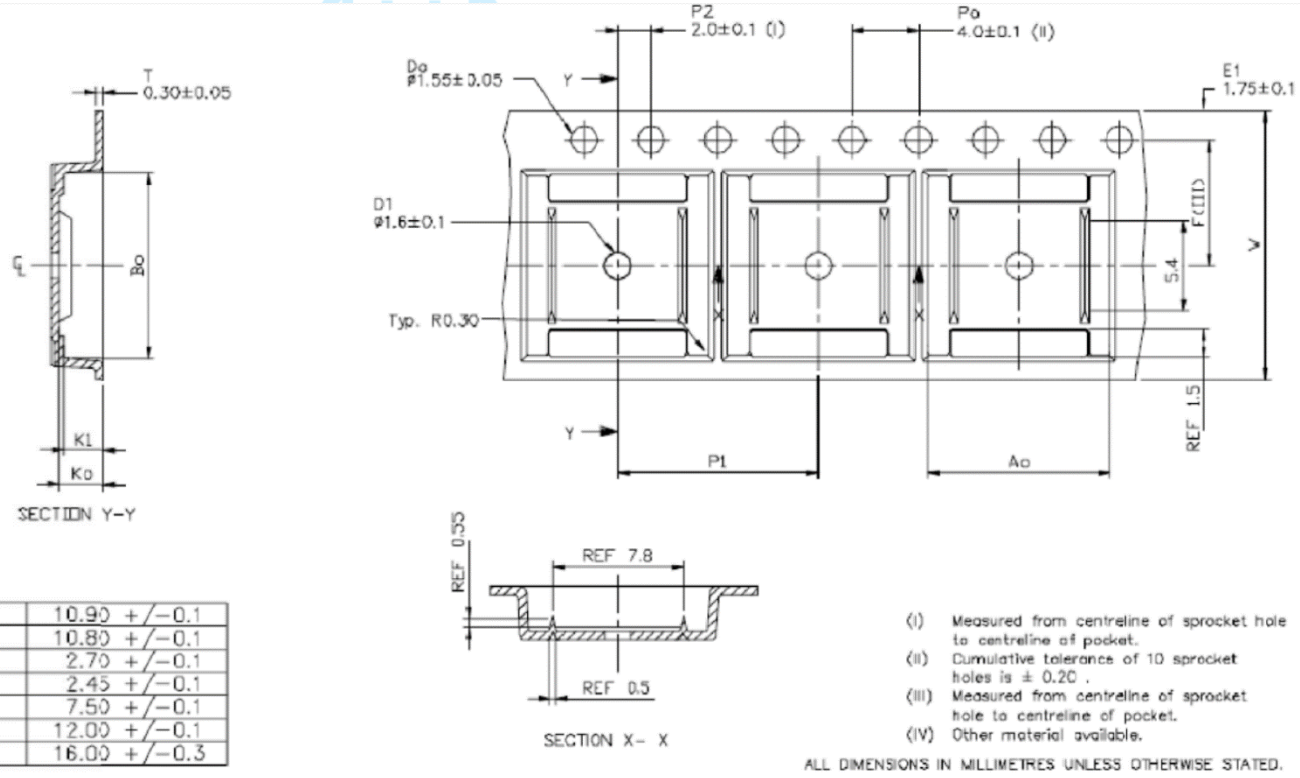
Figure16. 16-Lead Wide Body Outline Package [16-Lead SOIC_W]

REEL INFORMATION

8-Lead SOIC_N



16-Lead SOIC_W

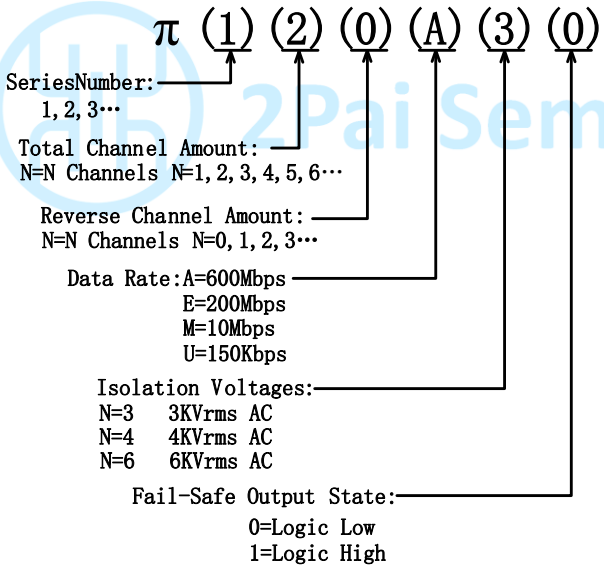


Ao	10.90 +/−0.1
Bo	10.80 +/−0.1
Ko	2.70 +/−0.1
K1	2.45 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

ORDERING GUIDE

Model Name		Temperature Range	No. of Inputs, V_{DD1} Side	No. of Inputs, V_{DD2} Side	Withstand Voltage Rating (kV rms)	Fail-Safe Output State	Package Description	Package Option	Quantity
π120A31	Pai120A31	−40°C to +125°C	2	0	3	High	8-Lead SOIC_N	S-8-N	4000 per reel
π120A30	Pai120A30	−40°C to +125°C	2	0	3	Low	8-Lead SOIC_N	S-8-N	4000 per reel
π121A31	Pai121A31	−40°C to +125°C	1	1	3	High	8-Lead SOIC_N	S-8-N	4000 per reel
π121A30	Pai121A30	−40°C to +125°C	1	1	3	Low	8-Lead SOIC_N	S-8-N	4000 per reel
π122A31	Pai122A31	−40°C to +125°C	1	1	3	High	8-Lead SOIC_N	S-8-N	4000 per reel
π122A30	Pai122A30	−40°C to +125°C	1	1	3	Low	8-Lead SOIC_N	S-8-N	4000 per reel
π120A61	Pai120A61	−40°C to +125°C	2	0	6	High	16-Lead SOIC_W	S-16-W	1000 per reel
π120A60	Pai120A60	−40°C to +125°C	2	0	6	Low	16-Lead SOIC_W	S-16-W	1000 per reel
π121A61	Pai121A61	−40°C to +125°C	1	1	6	High	16-Lead SOIC_W	S-16-W	1000 per reel
π121A60	Pai121A60	−40°C to +125°C	1	1	6	Low	16-Lead SOIC_W	S-16-W	1000 per reel
π122A61	Pai122A61	−40°C to +125°C	1	1	6	High	16-Lead SOIC_W	S-16-W	1000 per reel
π122A60	Pai122A60	−40°C to +125°C	1	1	6	Low	16-Lead SOIC_W	S-16-W	1000 per reel

PART NUMBER NAMED RULE



Notes:
Pai12xxxx is equals to π12xxxx in the customer BOM

REVISION HISTORY

Revision	Updated	Date	Page	Change Record
1	Jason	2018/09/19	All	Initial version
2	Jason	2018/11/28	P10	Changed the recommended bypass capacitor value from between 0.1 µF and 1 µF to between 0.1 µF and 10 µF.